

### IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, all pending claims are included below.

1. (Currently Amended) A device comprising:

a substrate ~~that has~~having a first conductivity type region ~~and, wherein the substrate has~~  
inwardly concaved recesses; ~~wherein the recesses have an~~ inwardly concaved geometry with  
having inflection points;

a gate dielectric formed on the first conductivity region of the substrate between the  
recesses;

a gate electrode formed on said gate dielectric, said gate electrode having a lower  
portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate  
electrode; and

a first silicon or silicon alloy layer in the inwardly concaved recesses that ~~form~~ forms a  
pair of inwardly concaved source/drain regions of a second conductivity type having extensions  
at the inflection points having a concentration of impurities in a range of  $1 \times 10^{16}/\text{cm}^3$  to  
 $3 \times 10^{21}/\text{cm}^3$  on opposite sides of said gate electrode, wherein the pair of inwardly concaved  
source/drain regions have an abrupt junction between the first conductivity type region and the  
first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points,  
wherein the pair of the inwardly concaved source/drain regions have extensions at the inwardly  
concaved geometry with the inflection points that is determined by the inwardly concaved  
recesses creating metallurgical inflection points directly beneath said lower portion of said gate  
electrode formed directly on said gate dielectric layer, ~~wherein said silicon or silicon alloy~~

source/drain regions extend the greatest distance laterally beneath said lower portion of the gate electrode at said inflection points, which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-100Å beneath said gate dielectric, and directly define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

2. (Previously Presented) The device of claim 1 wherein said silicon or silicon alloy source/drain regions extend above said gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric.

3. (Previously Presented) The device of claim 1 wherein said gate dielectric layer is thicker beneath outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode.

4. (Previously Presented) The device of claim 2 wherein said gate dielectric layer is thicker beneath said sidewall spacer and said outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode

5. (Currently Amended) The device of claim 1 further comprising a pair of a second silicon or silicon alloy regions layer having a first conductivity type region formed in the recesses between said pair of silicon or silicon alloy first silicon or silicon alloy layer y source/drain regions of said second conductivity type and said first conductivity type region.

6. (Currently Amended) The device of claim 5 wherein the concentration of said second silicon or silicon alloy regions layer having has a concentration that is greater than the concentration of a first conductivity type is greater than the concentration of said first conductivity type region.

7. (Canceled).

8. (Previously Presented) The device of claim 1 wherein said first conductivity type is n-type conductivity and wherein said second conductivity type is p-type conductivity.

9. (Previously Presented) The device of claim 1 wherein said first conductivity type is p-type conductivity and wherein said second conductivity type is n-type conductivity.

10. (Canceled).

11. (Currently Amended) The device of claim 1 wherein the concentration of said first silicon or silicon alloy source/drain regions layer has a concentration of impurities of a second conductivity type is approximately in a range between  $1 \times 10^{18}/\text{cm}^3$  to  $3 \times 10^{21}/\text{cm}^3$  to  $4 \times 10^{21}/\text{cm}^3$ .

12. (Previously Presented) The device of claim 1 further comprising silicide formed on said silicon or silicon alloy source/drain regions.

13. (Currently Amended) A device comprising:

a substrate that has a first conductivity type region and inwardly concaved recesses; ~~wherein the recesses have an inwardly concaved geometry with~~having inflection points;

a gate dielectric formed on the first conductivity type region of the substrate between the recesses;

a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a silicon-germanium alloy layer having a second conductivity type in the inwardly concaved recesses that ~~form~~forms a pair of inwardly concaved source/drain regions having a concentration of impurities of second conductivity type in a range of  $1 \times 10^{18}/\text{cm}^3$  to  $3 \times 10^{21}/\text{cm}^3$  along on opposite sides of said gate electrode with extensions directly beneath said lower portion of said gate electrode having an abrupt junction between the silicon germanium alloy filling the inwardly concaved recesses at the inflection points and the first conductivity type region, wherein said silicon germanium alloy layer extends above the height of said gate dielectric layer wherein the top surface of said deposited silicon-germanium alloy is spaced further from said gate electrode than said silicon-germanium alloy adjacent to said gate dielectric.

14. (Previously presented) The device of claim 13 wherein said gate dielectric layer is thicker beneath said outside edges of said gate electrode than the gate dielectric beneath the center of the gate electrode.

15. (Currently Amended) A device comprising:

a substrate that has a first conductivity type region and inwardly concaved recesses, ~~wherein the recesses have an inwardly concaved geometry having~~ with inflection points;

a gate dielectric formed on the first conductivity type region of the substrate between the recesses;

a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a silicon-germanium alloy layer having a second conductivity type in the inwardly concaved recesses that ~~form~~ forms a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of  $1 \times 10^{18}/\text{cm}^3$  –  $3 \times 10^{21}/\text{cm}^3$  at opposite sides of said gate electrode with extensions directly beneath said lower portion of said gate electrode having an abrupt junction between the first conductivity type region and the silicon-germanium layer filling the inwardly concaved recesses at the inflection points, wherein the pair of the inwardly concaved source/drain regions have the inwardly concaved geometry with the extensions at the inflection points that is determined by the inwardly concaved recesses creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer and to define a first

channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.